REMARKS

Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Claims 1-3 stand rejected under 35 U.S.C. 112, first paragraph. This rejection arises because of a typographical error in the amended claims as set forth in the Amendment filed April 15, 2002. It was not intended to add new subject matter. The new subject matter arose only from the typographical error. The claims are now amended to correct the error in the April 15, 2002 Amendment.

In view of the foregoing, the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

Attached is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,
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Enclosure: Appendix

APPENDIX
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

1. (Twice Amended) A transistor comprising:

a device isolation film formed on a semiconductor substrate, the device isolation film having a groove therein that exposes a portion of the semiconductor substrate defining an active region and having a substantially vertical profile with respect to the exposed portion of the semiconductor substrate;

a gate electrode structure formed in the central portion of the active region, separated from the device isolation film, wherein the gate electrode structure comprises:

a stacked structure of a gate oxide film, a first gate electrode and a second gate electrode being formed on the semiconductor substrate;

an oxide layer formed on a side wall of the first gate electrode; and

a first nitride spacer formed on the oxide layer;

a second nitride spacer formed on the [oxide layer] side wall of the device isolation film;

lightly doped drain (LDD) regions formed in the active region of the semiconductor substrate on both sides of the gate electrode;

source/drain regions formed in the active region of the semiconductor substrate on both sides of the gate electrode; and

second and third insulating films filling and planarizing the space above the active region and between the gate electrode structure and the second nitride spacer.

End of Appendix